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<u>L12</u>	l2 and L11	0	<u>L12</u>
<u>L11</u>	l8 and L10	0	<u>L11</u>
<u>L10</u>	maintain\$ near3 cache near3 level	174	<u>L10</u>
<u>L9</u>	l5 and l8	6	<u>L9</u>
<u>L8</u>	fill\$ near4 rate	9707	<u>L8</u>
<u>L7</u>	l5 and L6	0	<u>L7</u>
<u>L6</u>	fill\$ near4 rate	3845	<u>L6</u>
<u>L5</u>	L4	59	<u>L5</u>

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<u>L4</u>	l2 and L3	80	<u>L4</u>
<u>L3</u>	711/\$.ccls.	22122	<u>L3</u>
<u>L2</u>	fill\$ near3 cache near3 level	115	<u>L2</u>
<u>L1</u>	6507562.pn.	2	<u>L1</u>

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**1 Design of a parallel vector access unit for SDRAM memory systems**

*Mathew, B.K.; McKee, S.A.; Carter, J.B.; Davis, A.;*

High-Performance Computer Architecture, 2000. HPCA-6. Proceedings. Sixth International Symposium on , 8-12 Jan. 2000

Pages:39 - 48

[\[Abstract\]](#)   [\[PDF Full-Text \(116 KB\)\]](#)   IEEE CNF

**2 Cache resident data locality analysis**

*Samdani, Q.G.; Thornton, M.A.;*

Modeling, Analysis and Simulation of Computer and Telecommunication Systems, 2000. Proceedings. 8th International Symposium on , 29 Aug.-1 Sept. 2000

Pages:539 - 546

[\[Abstract\]](#)   [\[PDF Full-Text \(688 KB\)\]](#)   IEEE CNF

**3 Allowing for ILP in an embedded Java processor**

*Radhakrishnan, R.; Talla, D.; John, L.K.;*

Computer Architecture, 2000. Proceedings of the 27th International Symposium on , 10-14 June 2000

Pages:294 - 305

[\[Abstract\]](#)   [\[PDF Full-Text \(1204 KB\)\]](#)   IEEE CNF

**4 An X86 microprocessor with multimedia extensions**

*Draper, D.A.; Crowley, M.P.; Holst, J.; Favor, G.; Schoy, A.; Ben-Meir, A.; Trull, J.; Khanna, R.; Wendell, D.; Krishna, R.; Nolan, J.; Partovi, H.; Johnson, M.; Lee, T.; Mallick, D.; Frydel, G.; Vuong, A.; Yu, S.; Maley, R.; Kauffmann, B.;*

Solid-State Circuits Conference, 1997. Digest of Technical Papers. 44th ISSCC., 1997 IEEE International , 6-8 Feb. 1997

Pages:172 - 173, 450

[\[Abstract\]](#)   [\[PDF Full-Text \(872 KB\)\]](#)   IEEE CNF

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**5 Reducing the replacement overhead in bus-based COMA multiprocessors**

*Dahlgren, F.; Landin, A.;*

High-Performance Computer Architecture, 1997., Third International Symposium on , 1-5 Feb. 1997

Pages:14 - 23

[\[Abstract\]](#) [\[PDF Full-Text \(1008 KB\)\]](#) [IEEE CNF](#)

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**6 Using memory-mapped network interfaces to improve the performance of distributed shared memory**

*Kontothanassis, L.I.; Scott, M.L.;*

High-Performance Computer Architecture, 1996. Proceedings. Second International Symposium on , 3-7 Feb. 1996

Pages:166 - 177

[\[Abstract\]](#) [\[PDF Full-Text \(1376 KB\)\]](#) [IEEE CNF](#)

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**7 Decoupled modified-bit cache**

*Takahashi, M.; Oba, N.; Kobayashi, H.; Nakamura, T.;*

Computers and Communications, 1996., Conference Proceedings of the 1996 IEEE Fifteenth Annual International Phoenix Conference on , 27-29 March 1996

Pages:136 - 143

[\[Abstract\]](#) [\[PDF Full-Text \(684 KB\)\]](#) [IEEE CNF](#)

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**8 An adaptive high-low water mark destage algorithm for cached RAID5**

*Young Jin Nam; Chanik Park;*

Dependable Computing, 2002. Proceedings. 2002 Pacific Rim International Symposium on , 16-18 Dec. 2002

Pages:177 - 184

[\[Abstract\]](#) [\[PDF Full-Text \(457 KB\)\]](#) [IEEE CNF](#)

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**9 Reliability hierarchies**

*Chen, P.M.; Lowell, D.E.;*

Hot Topics in Operating Systems, 1999. Proceedings of the Seventh Workshop on , 29-30 March 1999

Pages:168 - 173

[\[Abstract\]](#) [\[PDF Full-Text \(32 KB\)\]](#) [IEEE CNF](#)

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**10 Exploiting fine-grain thread level parallelism on the MIT multi-ALU processor**

*Keckler, S.W.; Dally, W.J.; Maskit, D.; Carter, N.P.; Chang, A.; Lee, W.S.;*

Computer Architecture, 1998. Proceedings. The 25th Annual International Symposium on , 27 June-1 July 1998

Pages:306 - 317

[\[Abstract\]](#) [\[PDF Full-Text \(332 KB\)\]](#) [IEEE CNF](#)

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